Impact of Harmonic Voltage Distortion on the Voltage Sag Behavior of Adjustable Speed Drives

K. Stockman, J. Desmet, and R. Belmans

***Abstract*—The behavior of adjustable speed drives under voltage sag conditions and supplied form non-sinusoidal voltage waveforms has received little attention in recent years. This paper shows that voltage harmonic distortion has a major impact on the drive behavior. The impact of voltage sag conditions, including harmonics is represented by means of voltage tolerance curves. To overcome the impact, a fast field weakening control scheme for field oriented induction motor drives is analyzed.**

***Index Terms*—Adjustable Speed Drives, Harmonics, Voltage Sag, Field weakening.**

I. Introduction

The behavior of adjustable speed drives (ASD) under voltage sag conditions has received a lot of attention over the last decade due to the high economic losses involved [1],[2]. The research mainly concentrated on the assessment of voltage tolerance curves for ASD's supplied by idealized pre-disturbance voltage waveforms [3]-[5]. The testing procedures used during such assessment are based on a voltage sag classification method of which the classification suggested by Bollen [6],[7] or a simple classification between balanced and unbalanced single phase and two phase sags are the most popular [3]. The results of these tests are normally presented as voltage tolerance curves assuming perfect sinusoidal voltages before and during the voltage sag. These curves are extremely useful to compare the vulnerability of different commercially available ASD's and to identify the tripping mechanisms of the equipment.

As a result of the still increasing number of non linear equipment the assumption of sinusoidal supply voltages is no longer guaranteed in industrial supply systems. Consequently, the use of voltage tolerance curves of drives tested with sinusoidal voltages to estimate the immunity level of a machine or an industrial plant in a correct way is not straightforward.

In this paper, the impact of voltage harmonics on the voltage sag behavior of ASD's with diode rectifiers is analyzed. A good understanding of the impact of voltage harmonics in supply voltage will result in better prediction of equipment behavior. In the first section, the topology of the ASD is discussed with respect to it's behavior under sag conditions. The European Standard EN50160 [8] describing voltage characteristics in public supply systems is used to serve as a reference when testing ASD's . In a second section, the impact of harmonic voltage distortion on a drive system with diode rectifier is analyzed. Finally, a control scheme with fast field weakening is used to reduce the impact of harmonics on the overall performance of an ASD under voltage sag conditions.

II. Theoretical Considerations

A. Configuration of an ASD with diode rectifier

ASD's with diode rectifiers are widely spread in industry. Figure 1 illustrates the typical topology consisting of a diode rectifier stage, an intermediate dc link and an inverter supplying the motor. In the dc link a capacitor C is used for flattening the dc voltage. Typical values for the capacitor of commercially available ASD's vary between 75 and 165 µF/kW. An inrush circuit is required to guarantee a safe start-up of the drive, avoiding high charging currents through both the diodes and the capacitor.

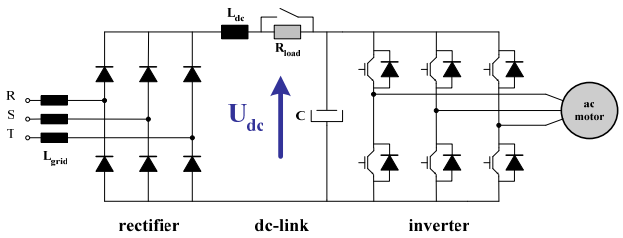

Figure 1: Configuration of an adjustable speed drive with diode rectifier.

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Under normal operation conditions, the dc link is charged six times each cycle. Consequently, the maximum dc link voltage U_{dc} will reach the maximum immediate value of the line voltage available at the input terminals of the ASD. When the dc link voltage is higher than the highest available line voltage, the dc link voltage starts to decay according to (1) with T_L being the load torque, ω_r the mechanical speed, η_{inv} the inverter efficiency and η_{mot} the motor efficiency.

$$U_{dc} C \frac{dU_{dc}}{dt} = \frac{T_L \omega_r}{\eta_{mot}\, \eta_{inv}} \quad (1)$$

At the occurrence of a balanced symmetrical three phase sag, no energy is supplied from the grid into the dc bus caused by the reverse biased diode rectifier. All energy needed to drive the load is taken from the energy stored in the dc bus capacitor *C*. To protect the ASD under such conditions, the undervoltage protection is monitoring the dc link voltage and will trip the drive to prevent damage to the diodes and capacitor at voltage recovery. The value of the undervoltage protection level $U_{dc\ Limit}$ differs a lot in commercially available ASD's. Some manufacturers even allow the customer to change this setting. In this case, the use of line chokes is required to prevent damage to the rectifier stage.

To protect the ASD for fast current transients and to reduce the harmonic content of the grid current, line chokes or a dc bus choke are frequently used. Typical values for the line chokes vary between 1 % and 5 % of the base impedance of the drive.

Using line chokes causes additional non-sinusoidal voltage drops over these elements. The resulting line voltage at the terminals of the drive rectifier is modified resulting in a slower current build up in the diodes and an increased conduction time. In Figure 2, the impact of a 3 % line choke on the dc bus voltage U_{dc} is illustrated (black line) for a 4 kW drive system supplied by a sinusoidal line voltage. Compared to the idealized situation with no grid impedance at all, a reduction of 4.9 % in the dc link voltage is noticed. In this paper, the impedance of the line chokes will be considered as a part of the grid impedance. The voltages at the terminals of the rectifier stage of the ASD will be taken as reference.

B. European Standard EN 50160

The European standard EN 50160 describes the voltage characteristics at the customer's supply terminals in public low voltage and medium voltage electricity distribution systems [8]. According to this standard the Total Harmonic Distortion factor (THD) should be less or equal to 8 % with respect to the fundamental voltage. Furthermore, limits are given for individual harmonic voltage components. No information on the phase angle of the harmonic voltages is given. Figure 3 shows the impact of the harmonic phase angle on the resulting line voltage amplitude for both fifth (solid line) and seventh (dashed line) harmonic voltage component for the maximum allowed harmonic voltages according to EN 50160, respectively 6 % and 5 %. In case of a fifth harmonic of 6%, line voltage amplitude will vary between 95 % and 106 % of rated voltage depending on the phase angle.

It can be concluded that the harmonic phase angle has a major impact on the amplitude of the resulting line voltage. As a consequence, phase angle information is required when analyzing the behavior of ASD's with diode rectifiers exposed to pre-disturbance voltages with harmonic content. Unfortunately, this phase angle information is not always available from measuring reports.

Figure 4 shows the waveform of the line voltage at the equipment terminals in a large Belgian company. The large amount of ASD's and other equipment with diode rectifiers within this production facility results in a significant reduction

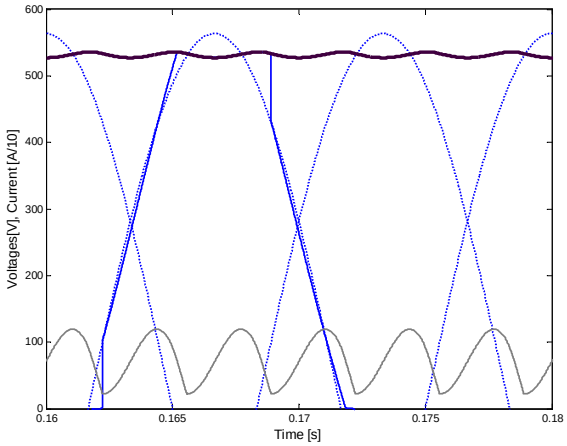

Figure 2: Reduction of dc bus voltage U_{dc} (black solid line) for an ASD with a 3 % line choke and supplied by a sinusoidal voltage (C = 145 µF/kW ; U_{line} = 400 V_{rms} ; P = 4 kW).

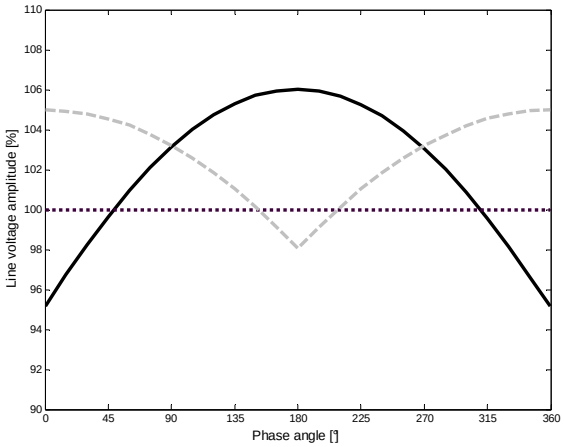

Figure 3: Impact of harmonic phase angle of fifth (6 %, solid line) and seventh (5 %, dashed line) voltage harmonic on the amplitude of the resulting line voltage.

of the voltage amplitude. The THD of this waveform is 3.5 %. A reduction of 5 % in the voltage amplitude with respect to a sinusoidal supply voltage can be noticed. In Table 1, the relative voltage and phase angle of each individual voltage harmonic is given. The voltage waveform in Figure 4 contains no triple order harmonics.

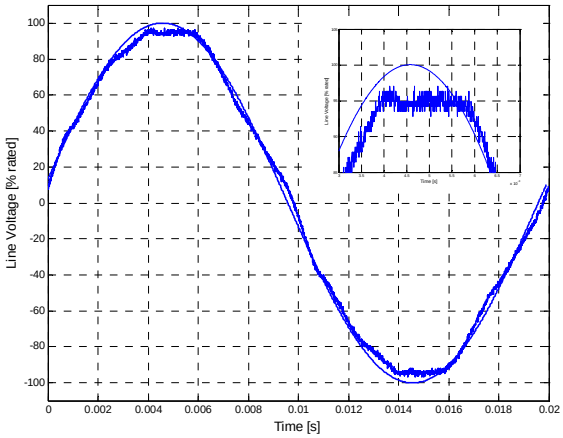

Figure 4: Typical line voltage waveform in a large Belgian company with a high number of ASD's with diode rectifier (THD = 3.5 %).

Table 1: Relative line voltage and phase angle for the harmonics at the equipment terminals in a large Belgian company according to Figure 4 (THD = 3.5 %).

Harmonic order	Relative voltage	Phase angle
5	2.6 %	- 172°
7	1.9 %	+ 140°
11	1.2 %	- 130°
13	0.7 %	+ 70°
17	0.1 %	- 145°

III. Commercial Adjustable Speed Drives

The impact of the line voltage presented in Figure 4 on the behavior of the dc link voltage is compared to the idealized situation of a perfect sinusoidal supply voltage and no grid impedance present.

Figure 5 shows the resulting dc link voltages before and during a 50 % voltage sag for a 4 kW field oriented drive running an induction motor at rated load and rated speed. The undervoltage protection level on the dc bus voltage is set at 75 % of rated value (dashed line). Due to the flattening effect of the harmonic voltages on the voltage amplitude, the maximum value of Udc is lower than in case of sinusoidal supply. It is also noticed that not all diodes contribute in the same amount to the charging of the dc link capacitor. At time 0.1 s, a balanced voltage sag with 50 % remaining voltage is initiated (Figure 5). During the sag, the relative voltage waveform harmonic content is not changed. The diodes are immediately reverse biased and the dc link voltage drops rapidly as the load has to be fed only by the energy in the dc link capacitor. If the undervoltage protection is not active, a new stable operating point is reached as soon as U_{dc} drops below the remaining grid voltage. The dc voltage ripple is increased compared to the pre-sag voltage ripple because the load power demand is kept constant.

If the undervoltage protection is activated, the ASD trips as soon as the limit threshold $U_{dc\ Limit}$ is crossed. The results for different values of remaining voltage and sag duration are presented in the voltage tolerance curve of Figure 6. For short interruptions and sags with low remaining voltage, increased vulnerability for ASD's supplied by distorted voltage waveforms compared to idealized voltage supply is noticed (vertical part of the voltage tolerance curve).

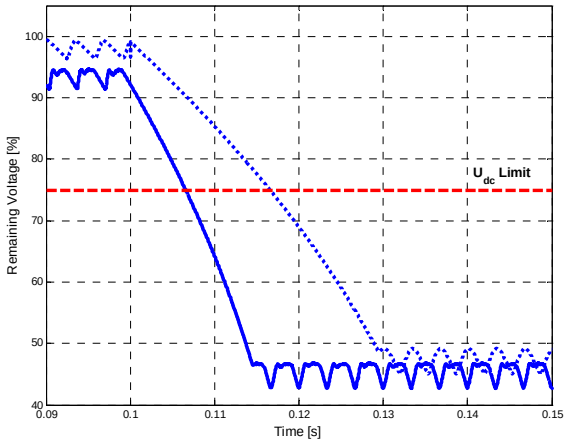

Figure 5: Dc link voltage U_{dc} behavior for a 50 % balanced voltage sag with sinusoidal supply voltage (dotted line) and voltage profile according to Figure 4 (solid line) with constant dc link load, (C = 145 µF/kW, $U_{dc\ limit}$ = 75 %, 4 kW load).

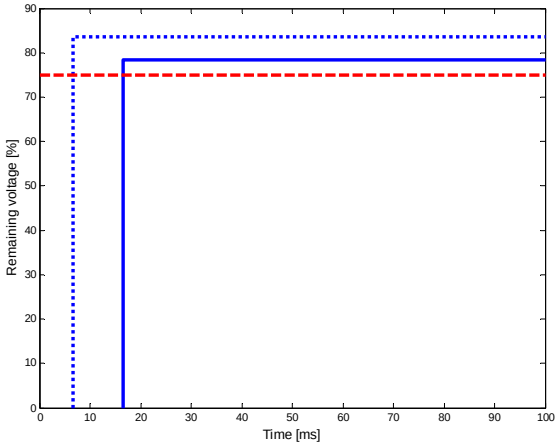

Figure 6: Voltage tolerance curve for both sinusoidal (solid line) and non sinusoidal supply voltage (dotted line), (C = 145 µF/kW, $U_{dc\ limit}$ = 75% (dashed line), 4 kW load).

Also for sags with high remaining voltage a significant increase in vulnerability is detected (horizontal part). For the voltage waveform of Figure 4 with a THD of 3.5 % and harmonic voltages as in Table 1, the horizontal part of the voltage tolerance curve is shifted for 5 % compared to idealized voltage supply.

From these observations, it can be concluded that the THD factor is not a good parameter to predict the impact of voltage harmonics on the behavior of ASD's subjected to voltage sags. The reduction of the line voltage amplitude compared to the rated value on the other hand is more suited to correct existing voltage tolerance curves generated with idealized supply voltage waveforms. Since this is not a suitable way of working, a more convenient parameter, the voltage crest factor (2) can be used.

$$CF(U) = \frac{U_{peak}}{U_{RMS}} \tag{2}$$

IV. CONTROL SCHEME WITH FAST FIELD WEAKENING

The main impact of typical harmonic voltage distortion is a reduction of the pre-sag dc link voltage U_{dc}. This causes increased sensitivity of ASD's compared to idealized supply characteristics as discussed in the previous section. In this section, a method to immunize an ASD for balanced sags is described.

The operation of a drive system operating at reduced dc bus voltage can be compared to a drive operated at high speed in field weakening mode. Under steady state conditions, the stator voltage equations of the induction machine can be simplified as all derivatives can be set zero and the magnetizing current i_μ can be replaced by the stator current component i_{sd}:

$$u_{sd} = R_s i_{sd} - \omega_\mu \sigma L_s i_{sq} \tag{3}$$

$$u_{sq} = R_s i_{sq} + \omega_\mu L_s i_{sd} \tag{4}$$

The electromagnetic torque T_{el} becomes:

$$T_{el} = p \frac{L_{1h}^2}{L_r} i_{sd} i_{sq} \tag{5}$$

If the drive is operated at a reduced dc bus voltage, the maximum available torque depends on the current and voltage limits within the drive. The maximum current I_{max} is set to 150% of the rated drive current i_{rated} (modern IGBT-modules can handle this maximum current for several seconds). The voltage limit U_{max} depends on the PWM-method used and the available dc bus voltage. Current and voltage limits are:

$$i_{sd}^{\ 2} + i_{sq}^{\ 2} \le 3 I_{\max}^{\ 2} \tag{6}$$

$$u_{sd}^{\ 2} + u_{sq}^{\ 2} \le \frac{3}{2} U_{\max}^2 \tag{7}$$

The basic idea of the control scheme is to set the magnetizing current as a function of the rotor speed and the available dc link voltage. In doing so, the ASD can operate at the maximum torque capability of the system [9]-[14]. As a result, the undervoltage protection level $U_{dc\ Limit}$ can be lowered compared to normal field oriented control. Thus, the reduced value U_{dc} caused by harmonic distortion can be counteracted by using this field weakening control scheme.

The implementation of the control scheme is based on simplified machine parameters, avoiding a voltage controller as is often suggested for field weakening operation for high speed applications (Figure 8). The magnetizing current set point i_μ^* is calculated as:

$$i_\mu^* = \sqrt{\frac{\frac{3}{2}\left(\frac{\hat{U}_{\max}}{\omega_\mu}\right)^2 - \left(L_s' I_{\max}\right)^2}{L_s^2 - L_s'^2}} \tag{8}$$

The use of a voltage controller for counteracting voltage sags would result is extra time delay before really adjusting the magnetization of the machine [9].

In Figure 7, the impact of the control scheme with fast field weakening on the voltage tolerance curves is illustrated. For a dc link voltage of 70 % of rated value, the ASD can still provide 95 % of rated torque for several seconds, depending on the overload capacity of the IGBT's in the inverter stage.

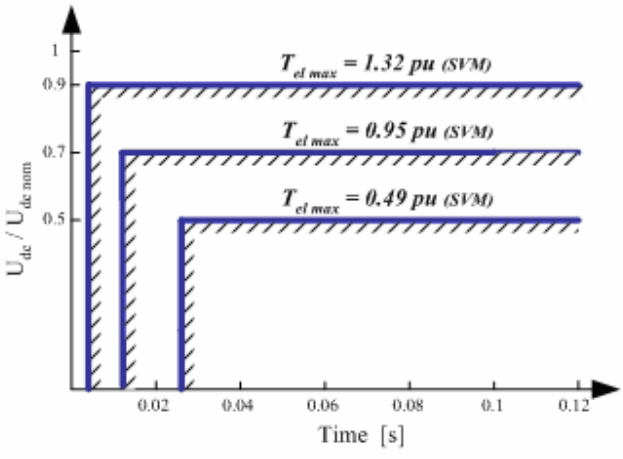

Figure 7: Voltage tolerance curves for a field oriented induction motor drive with fast field weakening control scheme.

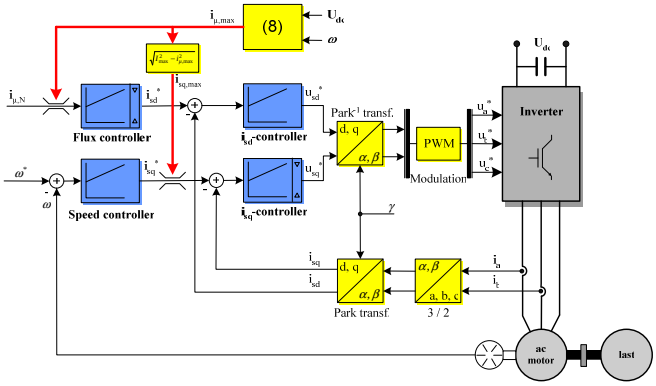

Figure 8: Control scheme with fast field weakening based on simplified machine equations.

V. Conclusion

In industrial applications, most ASD's are not supplied with sinusoidal voltages. Most voltage tolerance curves however are recorded using perfect sinusoidal voltage waveforms. This paper shows that the impact of harmonic distortion on the voltage tolerance curve can not be neglected. It is also shown that information on the phase angle of the harmonic voltage components is required to reconstruct the original voltage waveform to perform lab test on ASD's. The total harmonic distortion has shown to be an unreliable parameter to predict the behavior of an ASD. The crest factor on the other hand can be used to modify existing voltage tolerance curves generated with sinusoidal supply voltages. Finally, the impact of a control scheme with fast field weakening on the drive behavior is discussed. The control scheme proves to be simple and is very well suited to overcome the impact of reduced dc link voltage due to voltage distortion in the supply.

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